

FIG. 1

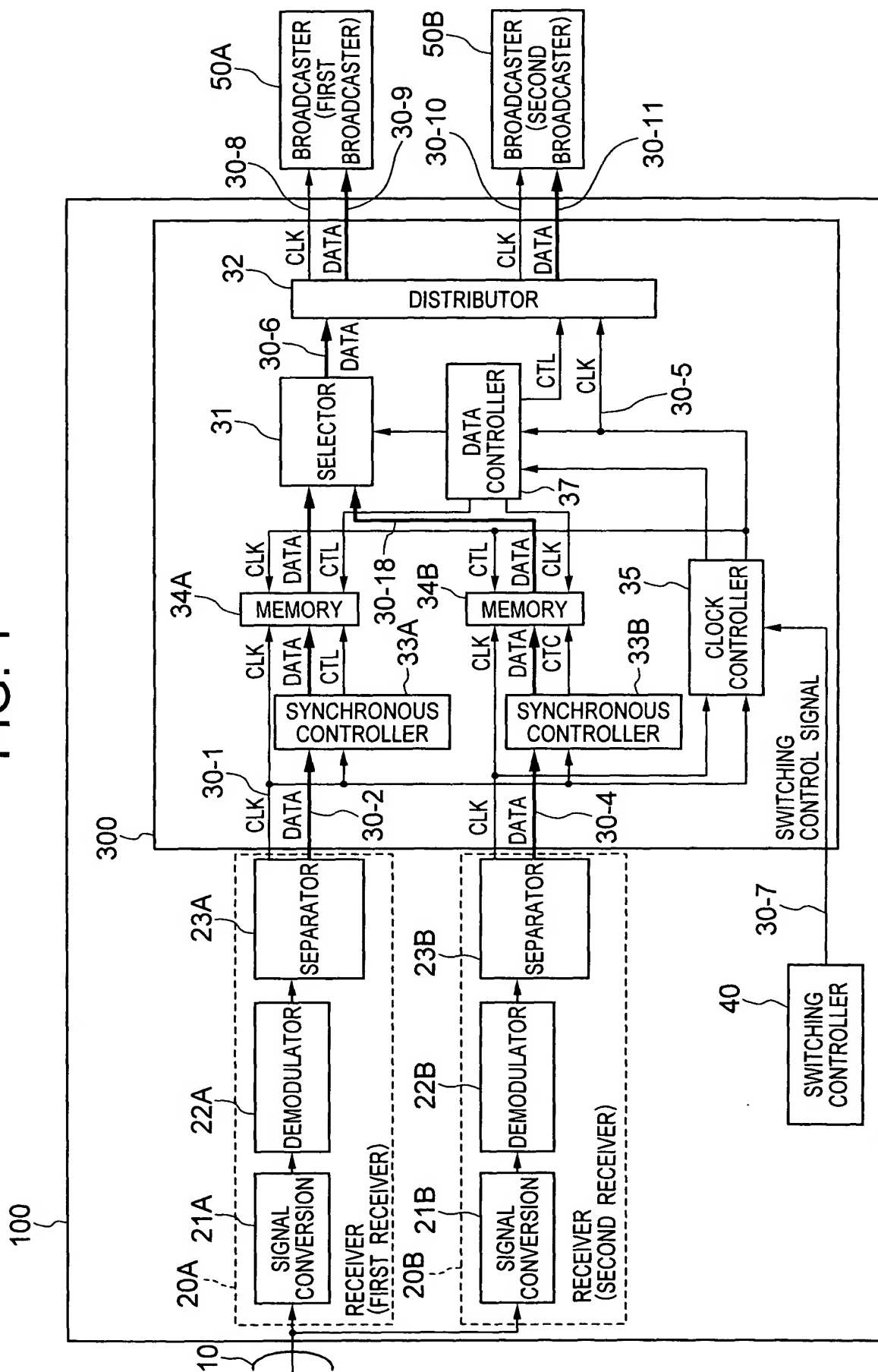
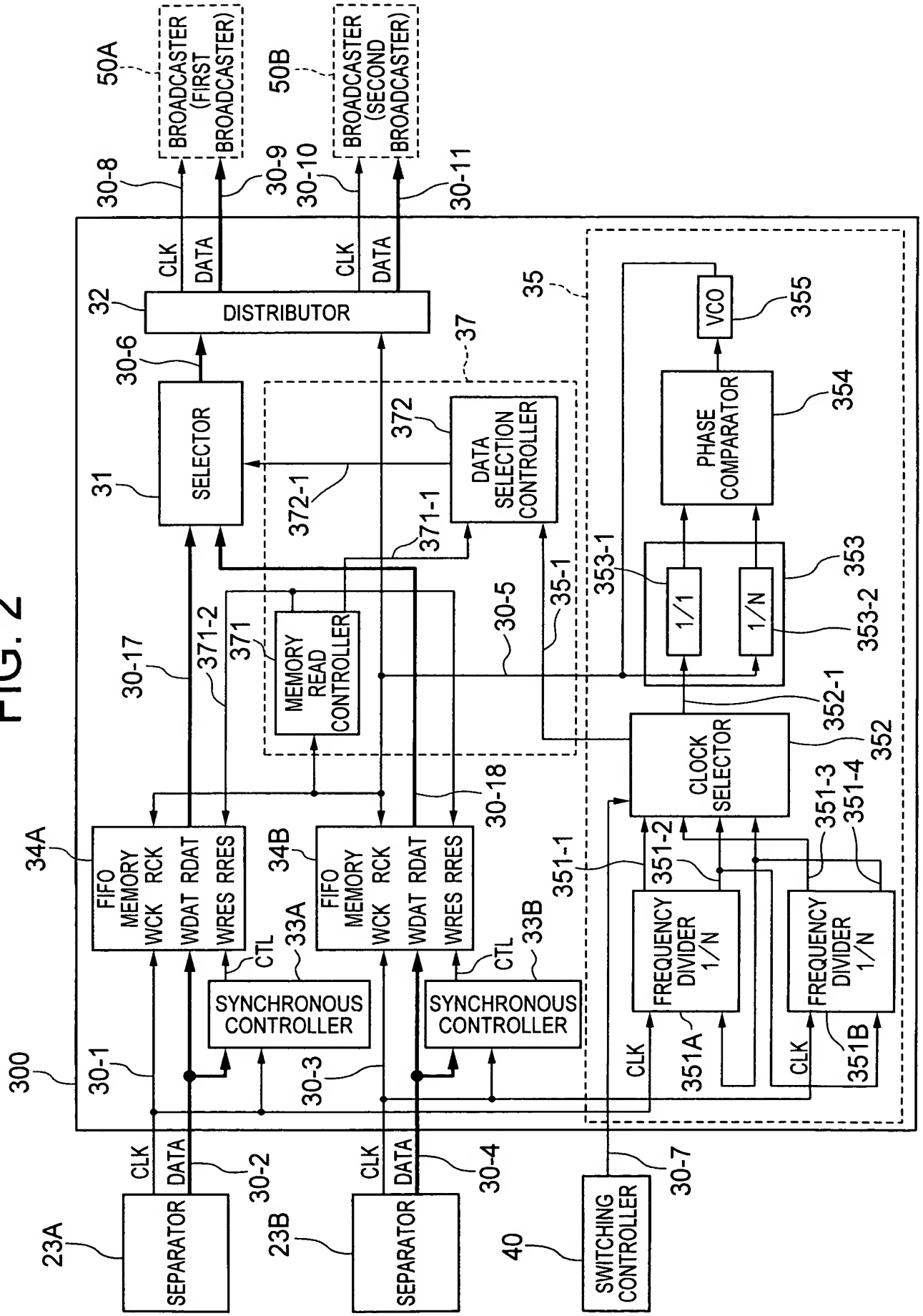


FIG. 2



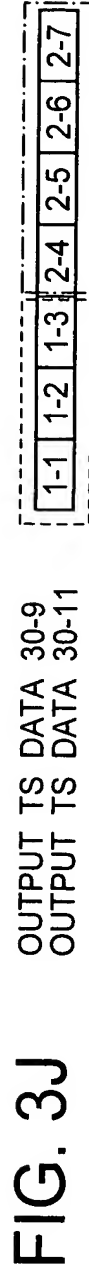
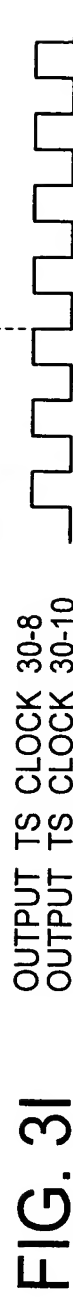
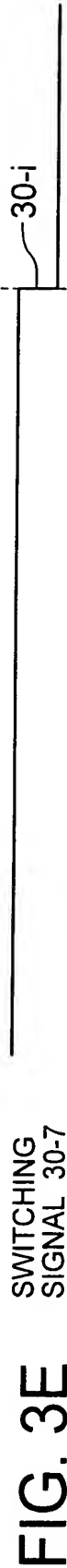
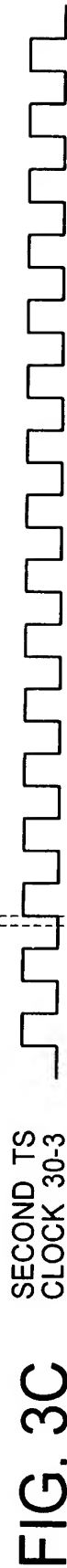
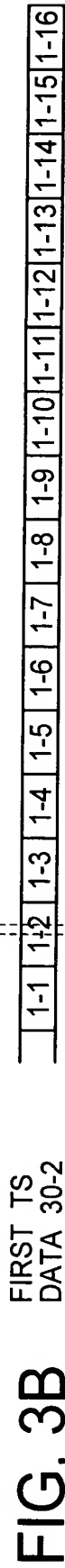
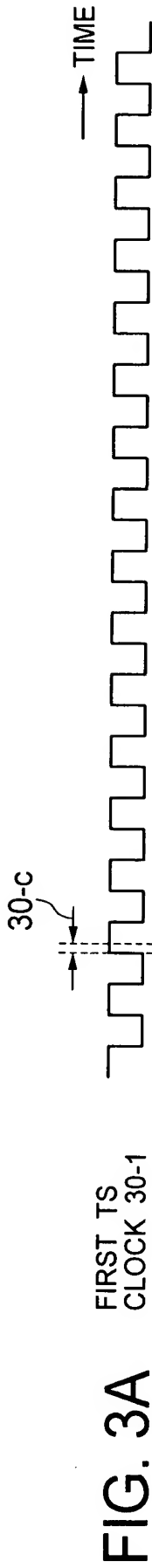
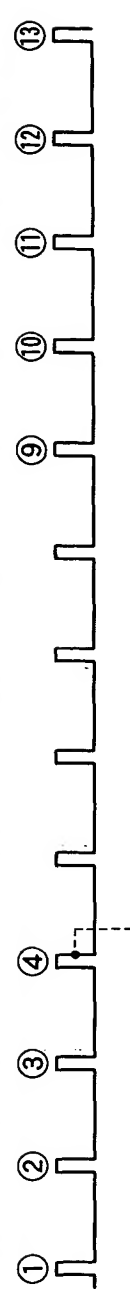
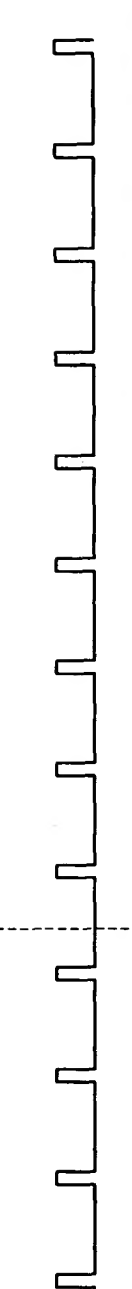




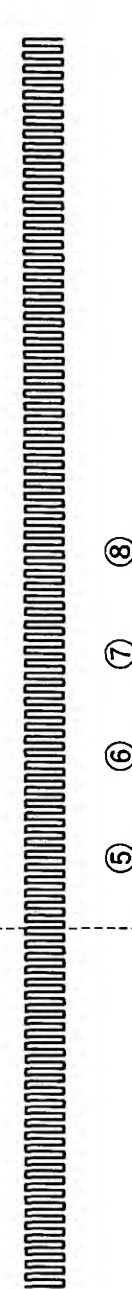
FIG. 4A



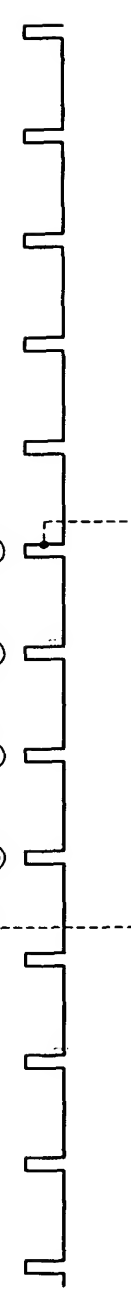
FIRST TS
FREQUENCY-DIVIDED CLOCK
351-1



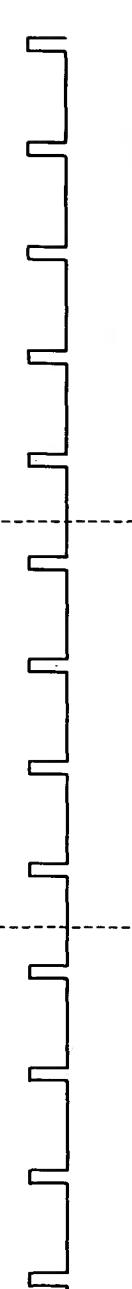
SECOND TS
FREQUENCY-DIVIDED RESET
351-2



SECOND TS
CLOCK 30-3



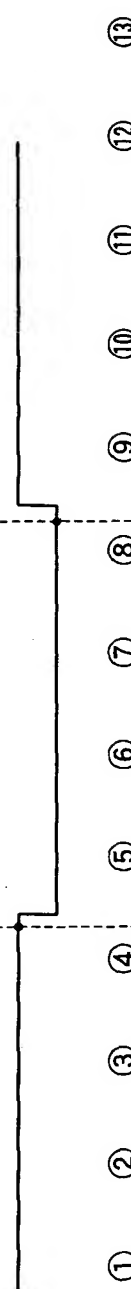
SECOND TS
FREQUENCY-DIVIDED CLOCK
351-3



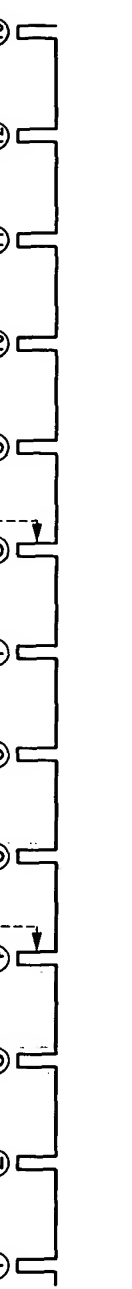
FIRST TS
FREQUENCY-DIVIDED RESET
351-4



SWITCHING
SIGNAL 30-7



SWITCHING
SIGNAL
(352 INTERNAL
SIGNAL)



SECOND TS
FREQUENCY-DIVIDED CLOCK
352-1

FIG. 4I

FIG. 4J VCO OUTPUT 355-1



FIG. 4K VCO FREQUENCY-DIVIDED CLOCK 353-2



FIG. 4L CLOCK SELECTOR OUTPUT 352-1



FIG. 4M INPUT 353-1 TO PHASE COMPARATOR

